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AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of fabricating trench isolation structures between integrated electrical devices in a semiconductor substrate, comprising:

placing a semiconductor substrate in a reaction chamber, the semiconductor substrate comprising trenches; and

completely filling the trenches with insulating material by atomic layer deposition, comprising a plurality of primary cycles, each primary cycle comprising, in sequence:

introducing a first vapor-phase reactant to the substrate, thereby forming no more than about one monolayer of a first reactant species conforming at least to surfaces of the trenches;

removing excess first vapor-phase reactant and byproduct from the reaction chamber;

introducing a second vapor-phase reactant to the substrate, thereby reacting with the first reactant species conforming at least to the surfaces of the trenches; and

removing excess second vapor-phase reactant and byproduct from the reaction chamber.

- 2. (WITHDRAWN).
- 3. (WITHDRAWN).
- 4. (WITHDRAWN).
- 5. (WITHDRAWN).
- 6. (Original) The method of Claim 1, wherein filling the trenches further comprises a plurality of secondary cycles, each secondary cycle comprising, in sequence:

introducing a third vapor-phase reactant to the substrate, thereby forming no more than about one monolayer of a third reactant species conforming at least to surfaces of the trenches, the third reactant species being different from the first reactant species;

removing excess third vapor-phase reactant and byproduct from the reaction chamber;

introducing a fourth vapor-phase reactant to the substrate, thereby reacting with the third reactant species conforming at least to the surfaces of the trenches; and



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removing excess fourth vapor-phase reactant and byproduct from the reaction chamber.

- 7. (Original) The method of Claim 6, wherein the first vapor-phase reactant comprises a silicon source gas, the third vapor-phase reactant comprises an aluminum source gas and the second and fourth vapor-phase reactants comprise oxidant source gases.
- 8. (Original) The method of Claim 7, wherein the aluminum source gas comprises alkyl aluminum compounds and the oxidant source gas comprises water.
- 9. (Original) The method of Claim 7, wherein filling the trench consists of mixing the primary cycle and secondary cycle in a primary cycle to secondary cycle ratio between about 20:1 and 1:10.
- 10. (Original) The method of Claim 6, wherein the primary cycles deposit a first oxide species and the secondary cycles deposit a second oxide species.
- 11. (Original) The method of Claim 10, wherein the first oxide species is silicon oxide and the second oxide species is a metal oxide.
- 12. (Original) The method of Claim 11, wherein the second oxide species is aluminum oxide.
- 13. (Original) The method of Claim 12, wherein filling the trench comprises depositing between about 23% and 37% aluminum oxide by weight in silicon oxide.
- 14. (Original) The method of Claim 12, wherein filling the trench comprises depositing between about 26% and 34% aluminum oxide by weight in silicon oxide
- 15. (Original) The method of Claim 10, wherein at least a portion of the first and second oxide species combine to form a separate phase in equilibrium with a portion of the first oxide.
- 16. (Original) The method of Claim 15, wherein the separate phase comprises mullite, the first oxide comprises silicon oxide and the second oxide comprises aluminum oxide.
- 17. (Original) The method of Claim 16, wherein the insulating material comprises between about 25% mullite and 50% mullite by weight.
- 18. (Original) The method of Claim 10, wherein the primary and secondary cycles are mixed in a ratio to match a coefficient of thermal expansion (CTE) of the insulating material to within about 20% of a CTE of the semiconductor substrate.

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19. (Original) The method of Claim 18, wherein the primary and secondary cycles are mixed in a ratio to match a coefficient of thermal expansion (CTE) of the insulating material to within about 10% of a CTE of the service. within about 10% of a CTE of the semiconductor substrate.